RECEIVED
CENTRAL FAX CENTER
JUL 12 2007

Docket No. 200314997-1

Remarks

This Amendment is responsive to the April 12, 2007 Office Action. Reexamination and reconsideration of **claims 1-24** is respectfully requested.

Summary of The Office Action

The specification has been objected to for the use of trademarked terms.

Claims 4, 12, 14, 16, 22, 23 and 14 have been objected to because of informalities.

Claims 7, 8, 13, 19 and 20 have been objected to under 35 U.S.C. §112, second paragraph, for the presence of trademarks or trade names in the claims.

Claim 11 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 11, 22, 23 and 24 have been rejected under 35 U.S.C. §101.

Claims 1-24 were rejected under 35 U.S.C. §102(b) as being anticipated by Bhatia et al. (US 6,535,798 B1).

Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatia et al. (US 6,535,798 B1).

RECEIVED
CENTRAL FAX CENTER
JUL 12 2007

Objections to the Specifications

The Office Action objects to the presence of trademarked terms in the specification. The items referred to by the trademarked terms are provided as examples of more generically identified items. Marking symbols have been added as suggested and thus paragraphs [0024], [0048], [0050] and [0053] have been amended to add the marks.

Objections to Informalities in the Claims

The Examiner's careful review of the claims is greatly appreciated. With the exception of the addition of the word "storage" into the preambles of claims 22 and 24, all of the informalities identified by the Examiner have been corrected. The definition of "computer-readable medium" has been amended. Further, addition of the word "storage" to the preambles of claims 22 and 24 is not required under current case law.

Applicant does not believe the scope of the claims has been changed since no new matter has been added.

Rejections under 35 U.S.C. 112, second paragraph

Claims 7, 8, 13, 19 and 20 was objected to under 35 U.S.C. §112, second paragraph, for the presence of trademarks or trade names in the claims. Claim 7 recites "TM2 register in a Pentium microprocessor", claim 8 recites "PROCHOT line available to a Pentium microprocessor", claim 13 recites a "Pentium 4 microprocessor", claim 19 recites "TM2 register in a Pentium microprocessor" and claim 20 recites "PROCHOT signal available to a Pentium microprocessor"

MPEP §2173.05(u) provides:

> **2173.05(u) Trademarks or Trade Names in a Claim**
>
> **The presence of a trademark or trade name in a claim is not, *per se*, improper under 35 U.S.C. 112, second**

Docket No. 200314997-1

> **paragraph**, but the claim should be carefully analyzed to determine how the mark or name is used in the claim. It is important to recognize that a trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. ... (Emphasis added).

Applicant respectfully submits that the use of the trademarked terms in claims 7, 8, 13, 19 and 20 is proper as the terms have been used in conjunction with the goods associated with the trademarks. Accordingly, claims 7, 8, 13, 19 and 20 particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Withdrawal of this rejection is respectfully requested.

Further, claim 11 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 11 has been amended to clarify the claim. The amendment is supported by, for example, the preamble of claim 11. Thus, no new matter has been added. The examiner's objections have been addressed and the rejection of claim 11 should be withdrawn. Accordingly, withdrawal of this rejection is respectfully requested.

The Claims Are Directed to Statutory Subject Matter

Claims 11, 22, 23 and 24 have been rejected under 35 U.S.C. §101 as being directed to non statutory subject matter.

Applicant submits that there is no rule or authority that states that intangible embodiments (or electrical signals) are non-statutory per se. In fact, the U.S. Patent Office's Board of Patent Appeals and Interferences has stated that physical subject matter includes both tangible and intangible matter, and include electrical signals. Ex parte Bilski, Board of Patent Appeals and Interferences, Appeal number 2002-2257, (Sept. 26, 2006), see pages 6, 17, 27, 37, and 38. The Examiner is requested to review the Bilski opinion since the current rationale for the rejection is contrary to case law and Patent Office holdings.

Claim 23 is directed to a common "system" claim and thus is statutory. First, all claimed elements are machine-implemented components or a manufacture. Thus the claim is one of the statutory categories of eligible subject matter in 35 U.S.C. §101: "machine," or "manufacture." Therefore, the rejection is improper. Second, even in embodiments that cover a general purpose computer that becomes a special purpose computer when programmed with the claimed elements, or a manufacture (e.g. a computer program embodied in a tangible medium which is capable of performing the claimed functions when executed by a machine), the claims involve a transformation of physical subject matter (which includes tangible or intangible matter). Ex parte Lundgren, 76 USPQ2d 1385, 1398-1399 (Bd. Pat. App. & Int. 2005) (precedential). For example, the "means for simulating a processor state" recites "writing a bit pattern to a logic." This involves a transformation of physical subject matter and thus the claim is statutory.

The Office Action notes that logic can be embodied as software and thus the claims are non-statutory. Applicant respectfully submits that no such statutory test exists and no case law supports such a conclusion. Rejections must be based on substantive law. MPEP 2107, I, first paragraph states, "Rejections will be based upon the substantive law..." No substantive law has been cited in the Office Action to support the 101 rejections and the rejections cannot stand.

Regarding claims 22 and 24, the definition of computer-readable medium has been amended. As such, withdrawal of this rejection is respectfully requested. Furthermore regarding computer-readable medium claims, MPEP 2106.01, Section I, paragraph 2, states:

> "In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See *Lowry*, 32 F.3d at 1583-84, 32 USPQ2d at 1035." (emphasis added)

For these additional reasons, the §101 rejection is contrary to the MPEP, case law, and Patent Office holdings. All claims define statutory subject matter and the rejection should be reversed.

The Claims Patentably Distinguish Over the References of Record

Claims 1-24 were rejected under 35 U.S.C. 102(b) as being anticipated by Bhatia et al. (US 6,535,798 B1). Bhatia is illustrated to be a conventional ACPI application that adds cyclic throttling. Bhatia does not disclose storing the GPIO block address or set of bit patterns to write to the GPIO block whose address is missing.

Independent claim 1

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1 recites a data structure that stores an address of a GPIO block and a set of bit patterns that may be written to the GPIO block or to a thermal management register. The reference does not disclose storing the address of the GPIO block or the set of bit patterns.

The Office Action asserts that Bhatia discloses the data structure being configured to store an address of a GPIO block:

> [instructions associated with software and/or applications include instructions for the loading/storing of information in the storage medium and as a result the instructions contain relative/absolute memory addresses or memory address pointers (Column 5, Line 9-11) the addresses can indicate a location on the "HOST BRIDGE" (Figure 1, 18) or "SYSTEM BRIDGE" (Figure 1, 34) for the loading/storing of data. "the location and structure of the control register may be defined under the ACPI object" (Column 12, line 51) and "The

> location and structure of the control register may be defined in memory or I/O address space (Column 12, 43) The examiner is equating I/O address space to a GPIO address]. Office Action at page 13.

The cited portions of Bhatia describe indication of a new performance state of a processor by writing a predefined value to a control register. (Bhatia, col. 12, lines 37-52). The cited portions of Bhatia do not teach a data structure configured to store an address of a GPIO block.

Claim 1 also recites "a logic ... to select a bit pattern ... selected from the set of bit patterns." The Office Action asserts that Bhatia discloses selecting a bit pattern at col. 11, lines 20-34, col. 9, line 46, and, col. 12, lines 24-30. The cited portions of Bhatia provide:

> A brief description of the interface signals between the power management control logic 100, 102 and the other components of the system follows. A signal VR_LO/HI# is provided by the control logic portion 100 to the voltage regulator 52 to adjust the voltage level supplied by the voltage regulator 52 up or down. A signal G_STPCLK# is provided to the processor 12 and a signal G_CPU_STP# is provided to the clock generator 50 to place the processor 12 in a low activity state (e.g., deep sleep or stop grant state) so that the clock frequency and supply voltage level of the processor 12 may be varied. The low activity state may also be defined as any of the C1, C2, and C3 states under the Advanced Configuration and Power Interface (ACPI) Specification, Revision 1.0, published on Dec. 22, 1996. Further, G_STPCLK# may be used to perform processor clock throttling. A signal LO/HI# provided by the control logic portion 100 to the processor 12 determines whether the core clock frequency of the processor 12 is at a high or low level. As an example, the core clock frequency may vary between 350 MHz and 450 MHz depending on whether LO/HI# is active or not. It is noted that additional signals may be used to adjust the core clock frequency to more than two levels. Similarly, additional signals other than VR_LO/HI# may also be used to control the voltage levels provided by the voltage regulator 52. In the illustrated embodiment, a signal G_LO/HI# from the system bridge 34, indicates the desired

Docket No. 200314997-1

> system state and controls the states of LO/HI# and VR_LO/HI#. (Bhatia, col. 11, lines 10-37).
>
> * * *
>
> In an alternative embodiment, more than two performance states may be defined... (Bhatia, col. 9, lines 46-47).
>
> * * *
>
> In addition, A BIOS routine may be used to respond to a generated power event. Other mechanisms are also possible.
>
> Referring to FIG. 8, the process executed by a power management module according to one embodiment in the system to control performance state transitions is illustrated. The power management module may be implemented as a software module, in system firmware (e.g., system BIOS or SMI handler), as part of the operating system, as a device driver, or as a combination of the above. The power management module determines (at 122) if a performance state change is required in response to a received event, indicating a thermal event, power supply transition, docking/undocking, a user command, or other event has occurred. The thermal event may be generated by one of the thermal arrangement routines (FIG. 2 or 3) described above. (Bhatia, col. 12, lines 24-33).

While these sections describe a conventional ACPI approach to power management through clock throttling, the sections do not describe selecting a bit pattern and writing the bit pattern to the GPIO block. Thus, Bhatia fails to teach each and every element of claim 1 and fails to establish a prima facie anticipation rejection. The rejection should be withdrawn.

Since claim 1 recites features not taught or suggested by the reference, it patentably distinguishes over the reference. Accordingly, dependent claims 2-10 also patentably distinguish over the reference and are in condition for allowance.

Independent claim 11

This claim recites a simulation logic to produce a simulated thermal management signal. The reference discloses only providing an actual thermal management signal. The claim also recites a combination logic that can selectively provide either an actual signal or a simulated signal. Once again the reference only discloses providing an actual thermal management signal.

The Office Action asserts that Bhatia discloses the combination logic:

> The power management module determines (at 122) if a performance state change is required in response to a received event, indicating a thermal event, power supply transition, docking/undocking, a user command, or other event occurred. (Bhatia, col. 12, lines 32-36).

Bhatia does not describe choosing between an actual signal and a simulated signal. Thus, this rejection is without basis and should be withdrawn.

Since claim 11 recites features not taught by the reference, it patentably distinguishes over the reference and is in condition for allowance. Accordingly, dependent claims 12-13 also patentably distinguish over the reference and are in condition for allowance.

Independent claim 14

Claim 14 is a method claim. Yet it is rejected by simply referring back to the rejection of claim 1, which is a system claim. This is improper and the rejection should be lifted on these grounds alone. Additionally, this claim refers to "simulation data" that facilitate controlling the state of a thermal management signal and a thermal management register. While the reference describes storing the fact that an interrupt occurred in a single register bit (Col. 4, line 4-6), it does not describe storing simulation data. For this additional reason this claim is not anticipated and is in condition for allowance.

RECEIVED
CENTRAL FAX CENTER
JUL 12 2007

Claims 15-21 depend from claim 14, which has been shown to be not anticipated by the reference. Thus, claims 15-21 are similarly not anticipated.

Independent claims 22 and 23

Claim 22 is directed to a computer-readable medium storing processor executable instructions operable to perform a method for simulating a processor performance state in a processor, the method comprising: receiving a request to establish the processor performance state in a the processor; accessing a data store to acquire simulation data that facilitates controlling a state of a thermal management signal and a thermal management register; and causing the processor performance state to be simulated by causing the processor to set its operating frequency and operating voltage in response to the thermal management signal produced in response to writing a bit pattern to a GPIO block. While the Office Action rejects claims 1 and 22-23 at pages 13-14 of the Office Action, the specific limitations of claims 22 and 23 are not addressed.

More specifically, claim 22 refers to "simulation data" that facilitate controlling the state of a thermal management signal and a thermal management register. While the reference describes storing the fact that an interrupt occurred in a single register bit (Col. 4, line 4-6), it does not describe storing simulation data. Additionally, claim 22 claims causing a processor state to be simulated in response to writing a bit pattern to a GPIO block. Bhatia does not describe writing anything to a GPIO block, let alone a bit pattern than can cause a processor to change its frequency and voltage. Thus, Bhatia fails to teach each and every element of the claim.

Accordingly, claim 22 is not anticipated and is in condition for allowance.

Independent claim 23

Claim 23 is directed to a system, comprising means for accessing addresses and bit patterns that facilitate controlling a thermal management signal available to a processor, where the processor is configured to selectively establish its operating frequency and

operating voltage based, at least in part, on the thermal management signal; means for receiving a request to place the processor into a processor performance state; and means for simulating the processor performance state by writing a bit pattern to a logic configured to control the thermal management signal. While the Office Action rejects claims 1 and 22-23 at pages 13-14 of the Office Action, the specific limitations of claims 22 and 23 are not addressed. Therefore, the rejection is improper for at least this reason and should be withdrawn.

Bhatia does not teach means for simulating the processor performance state by writing a bit pattern to a logic configured to control the thermal management signal. Thus, Bhatia fails to teach each and every element of the claim and the rejection should be withdrawn. Accordingly, claim 23 recites features not taught by the reference, it patentably distinguishes over the reference and is in condition for allowance.

Independent Claim 24

This claim is directed towards a set of application programming interfaces (API) embodied on a computer-readable medium for execution by a computer component. The API includes interfaces for communicating bit pattern data, GPIO bock address data, and state data. An API is well understood to provide access to a system to programmers. Using an API, a programmer can write a program to access a system. An API encapsulates the functionality of a system while exposing the functionality. Specification at [0054]-[0055].

The Office Action asserts that Bhatia discloses an API because "the power management module may be implemented as a software module, in system firmware (e.g., system BIOS or SMI handler), as part of the operating system, as a device driver, or as a combination of the above." (Bhatia, col. 12, lines 29-31). Applicant respectfully submits that Bhatia does not teach an API.

As discussed in greater detail above with respect to claim 1, Bhatia does not teach communicating a bit pattern data, communicating a GPIO block address data and/or

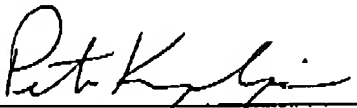
communicating a state data. Additionally, Bhatia does not teach state data that is related to a simulated processor performance state generated by applying the bit pattern data to a GPIO block identified by the GPIO block address data. Thus, Bhatia fails to teach each and every element of the claim and the rejection should be withdrawn.

Since claim 24 recites features not taught by the reference, it is in condition for allowance. Withdrawal of this rejection is respectfully requested.

Conclusion

For the reasons set forth above, **claims 1-24** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



Peter Kraguljac (Reg. No. 38,520)
(216) 348-5843
McDonald Hopkins LLC
600 Superior Avenue, E.
Suite 2100
Cleveland, OH 44114